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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,708	07/09/2003	Dong Suk Shin	CU-3283 RJS	9446

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,708	SHIN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 1 and 13 are objected to because of the following informalities:

Claim 1 recites the limitation "the substrate" in lines 5-6. The examiner respectfully suggests changing "the substrate" to --the **silicon** substrate-- in order to maintain proper antecedent basis and consistency throughout the claim language. Similar changes should be made in the rest of claim 1 and claim 13. Appropriate correction is required.

3. Claim 9 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 9 recites the limitation "The method of claim 9" in line 1. However, the dependency is improper.

Specification

4. The abstract of the disclosure is objected to because it does not contain of 150 words or less. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 7, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (US/5,792,695) in view of Ogura et al. (US/5,681,770).

Re claims 1 and 13, Ono et al. disclose a method for fabricating a semiconductor device, which comprises the steps of: depositing a gate electrode material film (i.e., conductive layer) (14A 14B) on a semiconductor substrate (11) and patterning the deposited gate electrode (conducive) material film so as to form a gate electrode (14A 14B) on the substrate (11); implanting impurity ions (i.e., n+ ions that planted to form 12 in the substrate 11) into the substrate (11) so as to form junction regions (12) in the substrate (11) (see Fig. 4; Col. 5, line 49 – Col. 6, line 3); forming an interlayer insulating film on the substrate and selectively patterning the interlayer insulating film so as to partially expose the surface of the substrate (see Col. 6, lines 4-12) ; and forming a two-layered contact plug consisting of a first contact layer (16) having high impurity concentration (i.e., the first layer **16** doped with $^{75}As+$ ion twice that will have higher concentration) (see Col. 6, lines 12-39) and a second contact layer (17) having low impurity concentration (i.e., the second layer **17** doped with $^{31}P+$ ion once and the will have

lower concentration impurity that n layer **16**) on the exposed surface of the substrate (11) and an insulating layer (14B and 22A) (see Ono et al. Figs. 4 and 5 and related text, Col. 5, line 49 – Col. 6, line 67).

Although it is conventional, Ono et al. do not specifically disclose forming of isolation regions (i.e., LOCOS isolation or STI isolation in the substrate).

Ogura et al. disclose a first step of the process entails forming field isolation regions (102) on substrate (104) (see Fig. 4A) by utilizing standard isolation processes, such as, LOCOS isolation or STI isolation in order to provide isolation between different active device forming regions (see Ogura et al. Col. 7, lines 15-28).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Ono et al. reference with forming of isolation regions in the substrate as taught by Ogura et al. in order to provide isolation between device formation active (i.e., transistor) regions.

Re claim 7, as applied to claim 1 above, Ono et al. and Ogura et al. disclose all the claimed limitations including the limitation wherein the first contact plug layer is formed of polycrystalline silicon or monocrystalline silicon see Ono et al. Figs. 4 and 5 and related text, Col. 5, line 49 – Col. 6, line 67; see Ogura et al. Col. 7, lines 15-28).

Re claim 16, as applied to claim 1 above, Ono et al. and Ogura et al. disclose all the claimed limitations including the limitation the step of implanting an impurity P or As into the exposed surface of the silicon substrate with implant dose $5.0x10^{15}$ cm^{-2} and implant energy 60 KeV (i.e., within the overlap range of the claimed range 10-100 KeV and a dose of 1E10-1E20

atoms/cm^3), after the step of treating the exposed surface (see Ono et al. Figs. 4 and 5 and related text, Col. 5, line 49 – Col. 6, line 67; see Ogura et al. Col. 7, lines 15-28).

Furthermore the implant concentration range activation energy range outside of the claimed limitations would have achieved by routine optimization. One of ordinary skill in the art would have been motivated to optimize the implant density range and activation energy range by using routine experimentation in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the implant density range and activation energy range by using routine experimentation, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed implant density and energy or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

7. Claims 2-6, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (US/5,792,695) and Ogura et al. (US/5,681,770), as applied to claim 1 in Paragraph 6 above, and in further view of Lin et al. (US/6,100,202).

Re claims 2-4, 14 and 15, as applied to claims 1 and 13 respectively in Paragraph 6 above, Ono et al. and Ogura et al. in combination disclose all the claimed limitations. However the combination do not disclose the step of treating the exposed surface of the silicon substrate by a process selected from the group consisting of a dry cleaning process, a wet cleaning process, a native oxide removal process, a thermal treatment process using hydrogen gas, and a surface treatment process using a laser.

Lin et al. disclose a method of fabricating semiconductor device the method includes forming a contact hole or via (45a 45b) by patterning the interlayer dielectric film (44a 44c) that deposited on the substrate (30) and after the contact hole formed the contact hole (opening) is cleaned using wet cleaning process independently used with the solution containing BOE (see Lin et al. Col. 11, lines 25-40) in order to remove residue or debris form the contact hole that was deposited during the etching process to form the contact opening.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Ono et al. and Ogura et al. reference with step of treating the exposed surface of the silicon substrate by a process selected from the group consisting of a dry cleaning process, a wet cleaning process, a native oxide removal process, a thermal treatment process using hydrogen gas, and a surface treatment process using a laser. as taught by Lin et al. in order to remove residue or debris form the contact hole that was deposited during the etching process to form the contact opening.

Furthermore, the temperature, the flow rate, duration of time and pressure used to clean the via can be done by routine optimization in order to get the desired the effective clean surface. One of ordinary skill in the art would have been motivated to optimize the temperature, the flow

rate, duration of time and pressure during cleaning of the via in order to get the desired the effective clean surface

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the temperature, the flow rate, duration of time and pressure used to clean the via, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed the temperature, the flow rate, duration of time and pressure or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claims 5, 6, as applied to claim 2 and above, Ono et al., Ogura et al. and Lin et al. in combination disclose all the claimed limitations including the step of implanting an impurity P or As into the exposed surface of the silicon substrate with implant dose $5.0x10^{15}$ cm^{-2} and implant energy 60 KeV (i.e., within the overlap range of the claimed range 10-100 KeV and a dose of 1E10-1E20 atoms/cm^3), after the step of treating the exposed surface (see Ono et al. Figs. 4 and 5 and related text, Col. 5, line 49 – Col. 6, line 67; see Ogura et al. Col. 7, lines 15-28).

Furthermore the implant concentration range activation energy range outside of the claimed limitations would have achieved by routine optimization. One of ordinary skill in the art would have been motivated to optimize the implant density range and activation energy range by using routine experimentation in order to achieve the desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the implant density range and activation energy range by using routine experimentation, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed implant density and energy or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

8. Claims 8-12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. (US/5,792,695) and Ogura et al. (US/5,681,770), as applied to claim 1 and 13 respectively in Paragraph 6 above, and in further view of Anderson et al. (US/5,916,369).

Re claims 8-12 and 17-19 as applied to claims 1 and 13 respectively in Paragraph 6 above, Ono et al. and Ogura et al. in combination disclose all the claimed limitations including

forming the first plug material comprises polysilicon and the second plug material comprises polysilicon.

However, the combination of Ono et al. and Ogura et al. do not specifically disclose wherein the first or second contact plug layer is deposited by atmospheric pressure chemical vapor deposition or low-pressure chemical vapor deposition using $DCS/H_2/PH_3$, $MS/H_2/PH_3$ or MS/PH_3 gas.

Anderson et al. disclose the LPCVD process that used a combination of precursor gases containing $DCS/H_2/PH_3$ in order to deposit doped polysilicon layer (see Anderson et al. Col. 1, line 65 – Col. 2, line 25).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Ono et al. and Ogura et al. reference with the LPCVD process that used a combination of precursor gases containing $DCS/H_2/PH_3$ as taught by Anderson et al. in order to deposit doped polysilicon layer.

Furthermore, the flow rate of DCS and H_2 gas and the pressure and the temperature to form the polysilicon layer and the PH3 content and flow rate and dopant dencity can be achieved by routine optimization. One of ordinary skill in the art would have been motivated to optimize the flow rate deposition temperature and pressure range by using routine experimentation in order to achieve the desired layer thickness and roughness and desired device performance.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to optimize the flow rate deposition temperature and pressure range by using routine experimentation, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by

routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed flow rate, temperature, pressure dopant concentration or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919, f.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure Nakajima et al. (5,397,724) and Hsu (US/6,171,954) also disclose similar inventive subject matter.

Correspondence

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

Brook Kebede

BK
March 19, 2005